

REMARKS

Claim Rejections 35 U.S.C. § 102 (a)

The Examiner has rejected claims 8, 10-12, and 14 under 35 U.S.C. §102 (a) as being anticipated by Matsumoto et al. (US 5,726,479, of record).

Applicant respectfully disagrees. The gate electrode of Applicant's claimed invention is not anticipated by the Matsumoto et al. reference cited by the Examiner.

The gate electrode of Applicant's claimed invention, as claimed in claim 8, as amended, comprises: a gate layer (320) disposed above a substrate (300), said gate layer (320) having a substantially level upper surface; a conductive layer (360) disposed over said gate layer (320); thin first spacers (330) disposed in contact with opposite sides of said gate layer (320) and below said conductive layer (360); and thick second spacers (340) disposed in contact with said thin first spacers (330), said thick second spacers (340) having a uniform width throughout its height. An embodiment of the gate electrode of Applicant's claimed invention is shown in Figure 3I.

In contrast, the gate electrode in the Matsumoto et al. reference cited by the Examiner has thick second spacers (7a) which do not have a uniform width throughout its height. Instead, the upper surface is severely rounded so the thick second spacers are not very thick at the top. See Figure 4 of Matsumoto et al. Failure to maintain a uniform width throughout the height of the thick second spacers will detrimentally affect (a) the implant profile of the lightly doped drain (LDD) below the sidewall structure, (b) the full separation between the salicide over the gate and the salicide over the source and drain necessary to prevent bridging and shorting, and (c) the integrity of the gate electrode as supported by the sidewall structure.

The gate electrodes of Applicant's claimed invention, as claimed in claims 10-12 and 14, are also not anticipated by Matsumoto et al. since claims 10-12 and 14 are dependent on claim 8, as amended.

Consequently, Matsumoto et al. fails to teach each and every element of Applicant's claimed invention. In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections under 35 U.S.C. §102 (a) to claim 8, 10-12, and 14.

Claim Rejections 35 U.S.C. § 102 (b)

The Examiner has rejected claims 8, 10-12, and 14 under 35 U.S.C. §102 (b) as being anticipated by Chen et al. (US 5,290,720, of record).

Applicant respectfully disagrees. The gate electrode of Applicant's claimed invention is not anticipated by the Chen et al. reference cited by the Examiner.

The gate electrode of Applicant's claimed invention, as claimed in claim 8, as amended, comprises: a gate layer (320) disposed above a substrate (300), said gate layer (320) having a substantially level upper surface; a conductive layer (360) disposed over said gate layer (320); thin first spacers (330) disposed in contact with opposite sides of said gate layer (320) and below said conductive layer (360); and thick second spacers (340) disposed in contact with said thin first spacers (330), said thick second spacers (340) having a uniform width throughout its height. An embodiment of the gate electrode of Applicant's claimed invention is shown in Figure 3I.

Just as in the gate electrode of Matsumoto et al. discussed in a previous section, the gate electrode in Chen et al. has thick second spacers (31) which do not have a uniform width throughout its height. Instead, the upper surface is severely rounded

so the thick second spacers (31) are not very thick at the top. See Figure 3 of Chen et al. As discussed in the previous section, failure to maintain a uniform width throughout the height of the thick second spacers will detrimentally affect (a) the implant profile of the lightly doped drain (LDD) below the sidewall structure, (b) the full separation between the salicide over the gate and the salicide over the source and drain necessary to prevent bridging and shorting, and (c) the integrity of the gate electrode as supported by the sidewall structure.

Furthermore, the gate electrode in the Chen et al. reference cited by the Examiner has thin first spacers (25) that are not disposed in contact with opposite sides of the gate layer (13). See Figure 3 of Chen et al.

The gate electrodes of Applicant's claims 10-12 and 14 are also not anticipated by Chen et al. since claims 10-12 and 14 are dependent on claim 8, as amended.

Consequently, Chen et al. fails to teach each and every element of Applicant's claimed invention. In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections under 35 U.S.C. §102 (b) to claims 8, 10-12, and 14.

CONCLUSION

Applicant believes that all claims pending, including amended claims 8, 10, 12, and 14, and new claim 123, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,

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Dated: 10/17, 2001



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VERSION WITH MARKINGS TO SHOW CHANGES MADE
IN THE CLAIMS

8. (Twice Amended) A gate electrode comprising:
 - a gate layer disposed above a substrate, said gate layer having a substantially level upper surface;
 - a conductive layer disposed over said gate layer, said conductive layer extending beyond edges of said gate layer;
 - thin first spacers disposed in contact with [adjacent to] opposite sides of said gate layer and below said conductive layer [wherein said thin first spacers have approximately the same height as said gate layer]; and
 - thick second spacers disposed in contact with [adjacent to each of] said thin first spacers, said thick second spacers having a uniform width throughout its height [, said thick second spacers comprising nitride, wherein said thick second spacers have approximately the same height as said gate layer; and
 - a conductive layer disposed over said gate layer, said conductive layer extending beyond edges of said gate layer].
10. (Twice Amended) The gate electrode of claim 8 [9] wherein said gate layer comprises polysilicon.
12. (Twice Amended) The gate electrode of claim 8 [11] wherein said thin first spacers comprise oxide.

13. (Twice Amended) The gate electrode of claim 11 [13] wherein said polycide comprises titanium salicide (TiSi₂).